REMARKS

Claim 22 has been objected to due to a noted informality. Claim 22 has been amended as suggested by the Examiner.

Claims 4 and 5 were rejected under 35 U.S.C. 103(a) as being unpatentable over Upp in view of Lincoln.

In claim 4, Applicants claim "reading, by the receiver block, of the data signal with a different sampling period than the transmission period of the transmitter block, wherein sampling by the receiver block for reading in accordance with the sampling period occurs simultaneously with reception by the receiver block of the synchro signal". Support for this amendment is provided as least by specification paragraph 44 which teaches that the receiver reads and recovers the data signals simultaneously with the reception of the synchro signal. The Examiner concedes that the use of a different sampling period is not taught by Upp, and instead cites to Lincoln. Lincoln teaches, for a given transmission line, multiple phase delay registers that are controlled by a clock circuit to sample at different sampling times (paragraph 49). The sampling operation, however, is driven by the receiver clock (Figure 6). There is no teaching or suggestion in Upp or Lincoln for having the clock driven sampling for reading (which is at a different sampling period than the transmission period) "occur[] simultaneously with reception by the receiver block of the synchro signal" in the manner claimed. Claim 4 is accordingly patentable over the cited prior art.

Claim 5 has been amended in a manner similar to claim 4. Applicants assert that claim 5 is patentable over the cited prior art for at least the same reasons as claim 4.

Claims 2, 3, 14, 16, 17, and 25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Upp in view of Cagenius.

Claim 2 has been amended to recite that "the second instant for sending said synchro signal for communication over the third line is delayed with respect to the first instant for sending the data signal for communication over the first line." The Examiner points to Cagenius with respect to the claimed delay. More specifically, the Examiner asserts that Cagenius teaches

that the "frame sync is delayed by a predetermined amount along with the data to ***preserve the timing relationship*** between the frame sync and the data" (emphasis added, Office Action page 6). This is different from the claimed invention. The amendments presented by Applicants emphasize that instant for sending the synchro signal is delayed with respect to the instant for sending the data signal. Cagenius instead imposes delays to both signals in the FIFO buffer 46 in order preserve their timing relationship to each other. It would thus appear that the instants of sending the data and synchro signals are the same in Cagenius, and this does not teach the delay between the claimed first and second instants as emphasized by claim 2.

Claim 14 has been amended to recite "delaying between a first instant for sending the data signal over the first communications line and a second instant for sending the synchronization signal over the second communication line." The claimed delay between the instants for sending of the data signal and sending of the synchronization signal is not taught or suggested by Cagenius. As noted by the Examiner, Cagenius teaches that the "frame sync is delayed by a predetermined amount ***along with the data***."

Claim 25 has been amended to recite that "an instant for sending of the active synchronization signal transmission over the third communication line is delayed after an instant for sending of the data signal transmission on the first communication line." Again, Cagenius does not teach or suggest that the instant for sending of the synch signal is delayed after the instant of sending of the data signal.

In view of the foregoing, Applicants submit that claims 2, 14 and 25 are patentable over the cited prior art.

Claims 6, 9, 10, and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Upp in view of the admitted prior art.

The Examiner has asserted the same argument for rejection as was previously presented in the April 4, 2009 Office Action. Applicants have previously responded to that argument. The current Office Action does not appear to address Applicants' arguments in favor of claims 6, 9, 10 and 19. Applicants accordingly repeat the same argument for patentability as was previously asserted and request that the Examiner respond to this argument.

Claim 6 includes limitations relating to repeater stages and elementary delays. The Examiner concedes that these features are not taught by Upp, but asserts that such are recognized as admitted prior art in the background of this application. Applicants do recognize the use of repeaters as being in the prior art, but Applicants do not admit that the elementary delay configuration in known from or is inherent in the admitted prior art. Applicants accordingly traverse the rejection and request that the Examiner prove, with respect to the admitted prior art, that the "stages have an elementary delay which must be shorter than half the transmission period." Applicants further assert that choosing such an elementary delay is not an obvious matter of design choice. Accordingly, Applicants request that the Examiner provide a reference teaching the selection of the claimed elementary delay.

Claims 9 and 19 also include limitations relating to repeater stages. However, Applicants specifically claim that the tristate condition of the data and syncho repeaters is controlled by the tristate output of the congestion repeater. The repeaters shown in admitted prior art Figure 1 do not teach using the specifically claimed configuration for controlling data/syncho repeaters with the congestion repeater. As such, the prima facie rejection has not been satisfied. Withdrawal of the rejection to claims 9 and 19 is requested.

In view of the foregoing, Applicants submit that claims 6, 9, 10, and 19 are patentable over the cited prior art.

Claims 22 and 23 were rejected under 35 U.S.C. 103(a) as being unpatentable over Upp in view of Hann.

The Examiner has asserted the same argument for rejection as was previously presented in the April 4, 2009 Office Action. Applicants have responded to that argument. The current Office Action does not appear to address Applicants' arguments in favor of claims 22 and 23. Applicants accordingly repeat the same argument for patentability as was previously asserted and request that the Examiner respond to this argument.

Claim 22 emphasizes the use of transmit/receive control lines in addition to data, synchro and congestion lines. The transmit/receive control lines specify which communications blocks are to function as transmitters and which are to function as receivers. Upp uses a bus arbitration

and assignment protocol to assign transmit/receive functions to users based on request. The Examiner points to Upp's clock and ack lines as being transmit and receive signal lines, respectively. While these may be signal lines used for transmitting and receiving, Applicants claim language is more precise.

Specifically, claim 22 previously recited that these signal lines carry "control signals" which "specify, for the bi-directional first communication line, which of the first and second communication blocks is a transmitter of the data signal and which of the first and second communication blocks is a receiver of the data signal." The clock line provided by Upp does not specify which of the blocks are to be the transmit and receive blocks with respect to a data signal. Likewise, the ack line provided by Upp does not specify which of the blocks are to be the transmit and receive blocks with respect to a data signal. The Examiner must consider all of the material claim limitations, and in this case the Examiner's technical analysis fails to prove the existence of signal lines in Upp which "specify, for the bi-directional first communication line, which of the first and second communication blocks is a transmitter of the data signal and which of the first and second communication blocks is a receiver of the data signal."

Claim 22 recites that "the first and second communications blocks ***set a logic state of the transmit signal line and receive signal line*** which specify, for the bi-directional first communication line, which of the first and second communication blocks is a transmitter of the data signal and which of the first and second communication blocks is a receiver of the data signal." The clock and ack lines in Upp are not set by the blocks to specify which block is to use the data line for transmission and which block is to use the data line for reception. Assignment of transmit/receive functionality in Upp is made through the bus arbitration and assignment protocol and the transmission of assignment data during a given clock cycle for a next frame (see, col. 4, lines 38-48). There is no signal line in Upp whose logic state is set to specify transmit/receive assignment.

In view of the foregoing, Applicants submit that claims 22 and 23 are patentable over the cited prior art.

Applicants respectfully submit that the application is now ready for allowance.

No fees are believed to be due at this time, however Applicants hereby authorize the Commissioner to charge any fees that may be required by this paper or credit any overpayment of fees to Deposit Account No. 07-0153.

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Respectfully submitted,

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